63 4-2

NEL REPORT 1161

MACOMATIC
CORRELATION SIGNAL PROCESSING SYSTEM

W. B. Allen and C. E. Persons

Research and Development Report 1161

14 March 1963

U. S. NAVY ELECTRONICS LABORATORY, SAN DIEGO, CALIFORNIA • A BUREAU OF SHIPS LABORATORY

INITIAL DISTRIBUTION LIST

CHIEF, BUREAU OF SHIPS
CODE 210L (8)
CODE 240C (2) -2-
CODE 320
CODE 360
CODE 370
CODE 670 (2) -2-
CHIEF, BUREAU OF NAVAL WEAPONS
DLI-3
DLI-31
R-56
RUDC-2
CHIEF OF NAVAL PERSONNEL
PERS 11B
CHIEF OF NAVAL OPERATIONS
OP-07T
OP-701E1
OP-03EG
CHIEF OF NAVAL RESEARCH
CODE 466
COMMANDER IN CHIEF US PACIFIC FLEET
COMMANDER IN CHIEF US ATLANTIC FLEET
COMMANDER OPERATIONAL TEST AND
EVALUATION FORCE
DEPUTY COMMANDER OPERATIONAL TEST -
EVALUATION FORCE, PACIFIC
COMMANDER CRUISER-DESTROYER FORCE,
US ATLANTIC FLEET
COMMANDER TRAINING COMMAND
US PACIFIC FLEET
COMMANDER SUBMARINE DEVELOPMENT
GROUP TWO
US NAVAL AIR DEVELOPMENT CENTER
NADC LIBRARY
US NAVAL MISSILE CENTER
TECH. LIBRARY, CODE NO 3022
US NAVAL ORDNANCE LABORATORY
LIBRARY
US NAVAL ORDNANCE TEST STATION
PASADENA ANNEX LIBRARY
US NAVAL ORDNANCE TEST STATION
CHINA LAKE
PORTSMOUTH NAVAL SHIPYARD
PUGET SOUND NAVAL SHIPYARD
SAN FRANCISCO NAVAL SHIPYARD (2) -2-
DAVID TAYLOR MODEL BASIN -2-
APPLIED MATHEMATICS LABORATORY (2) -2-
DAVID TAYLOR MODEL BASIN
/LIBRARY/
US NAVY MINE DEFENSE LABORATORY
USN UNDERWATER SOUND LABORATORY -3-
LIBRARY (3)
ATLANTIC FLEET ASW TACTICAL SCHOOL
USN ENGINEERING EXPERIMENT STATION
US NAVAL RESEARCH LABORATORY
CODE 2027
CODE 5120
USN UNDERWATER SOUND REFERENCE LAB.
BEACH JUMPER UNIT TWO
US FLEET ASW SCHOOL
USN UNDERWATER ORDNANCE STATION
OFFICE OF NAVAL RESEARCH
PASADENA
US NAVY HYDROGRAPHIC OFFICE (2) -2-
SUPERVISOR OF SHIPBUILDING US NAVY
GROTON
US NAVAL POSTGRADUATE SCHOOL -2-
LIBRARY (2) -2-
OFFICE OF NAVAL RESEARCH
BOSTON
ASSISTANT SECRETARY OF THE NAVY R-D
ONR SCIENTIFIC LIAISON OFFICER
WOODS HOLE OCEANOGRAPHIC INSTITUTION
DOD RESEARCH AND ENGINEERING
TECHNICAL LIBRARY
DEFENSE ATOMIC SUPPORT AGENCY
NASA -3-
LANGLEY RESEARCH CENTER (3) -3-
COMMITTEE ON UNDERSEA WARFARE
US COAST AND GEODETIC SURVEY
US BUREAU OF COMMERCIAL FISHERIES
WASHINGTON 25, D. C.
HONOLULU-JOHN C MARR
POINT LOMA STATION
WOODS HOLE,
ARMED SERVICES TECHNICAL
INFORMATION AGENCY (10)
ABERDEEN PROVING GROUND, MARYLAND
EDGEWOOD ARSENAL
UNIVERSITY OF MIAMI
THE MARINE LAB. LIBRARY (3) -3-
NEW YORK UNIVERSITY
DEPT OF METEOROLOGY - OCEANOGRAPHY
COLUMBIA UNIVERSITY
HUDSON LABORATORIES
LAMONT GEOLOGICAL OBSERVATORY
RUTGERS UNIVERSITY
FISHERIES-OCEANOGRAPHY LIBRARY
UNIVERSITY OF RHODE ISLAND
NARRAGANSETT MARINE LABORATORY
BROWN UNIVERSITY
THE UNIVERSITY OF TEXAS
DEFENSE RESEARCH LABORATORY
HARVARD UNIVERSITY

Navy Electronics Laboratory
Report 1161

MACOMATIC CORRELATION SIGNAL PROCESSING SYSTEM, by W. B. Allen and C. E. Persons 40 p., 14 March 1963.

UNCLASSIFIED

A magnetic core matrix time compressor (MACOMATIC) has been developed for incorporation into a pseudorandom-signal-correlation sonar system. The MACOMATIC features a highly flexible input sampling rate -- any rate of up to 400 bits per second -- and a storage capacity of 2048 bits. Special timing pulses in the core matrix permit Doppler correction by adding or subtracting bits of information to effectively compress or expand the stored signal. The MACOMATIC is recommended particularly for use with spectrum analyzers for investigating low and very-low frequency phenomena.

1. MACOMATIC
2. Sonar signals - Processing

I. Allen, W. B.
II. Persons, C. E.

SF 001 03 01, Task 8104
(NEL N1-1)

This card is UNCLASSIFIED

Navy Electronics Laboratory
Report 1161

MACOMATIC CORRELATION SIGNAL PROCESSING SYSTEM, by W. B. Allen and C. E. Persons 40 p., 14 March 1963.

UNCLASSIFIED

A magnetic core matrix time compressor (MACOMATIC) has been developed for incorporation into a pseudorandom-signal-correlation sonar system. The MACOMATIC features a highly flexible input sampling rate -- any rate of up to 400 bits per second -- and a storage capacity of 2048 bits. Special timing pulses in the core matrix permit Doppler correction by adding or subtracting bits of information to effectively compress or expand the stored signal. The MACOMATIC is recommended particularly for use with spectrum analyzers for investigating low and very-low frequency phenomena.

1. MACOMATIC
2. Sonar signals - Processing

I. Allen, W. B.
II. Persons, C. E.

SF 001 03 01, Task 8104
(NEL N1-1)

This card is UNCLASSIFIED

Navy Electronics Laboratory
Report 1161

MACOMATIC CORRELATION SIGNAL PROCESSING SYSTEM, by W. B. Allen and C. E. Persons. 40 p., 14 March 1963.

UNCLASSIFIED

A magnetic core matrix time compressor (MACOMATIC) has been developed for incorporation into a pseudorandom-signal-correlation sonar system. The MACOMATIC features a highly flexible input sampling rate -- any rate of up to 400 bits per second -- and a storage capacity of 2048 bits. Special timing pulses in the core matrix permit Doppler correction by adding or subtracting bits of information to effectively compress or expand the stored signal. The MACOMATIC is recommended particularly for use with spectrum analyzers for investigating low and very-low frequency phenomena.

1. MACOMATIC
2. Sonar signals - Processing

I. Allen, W. B.
II. Persons, C. E.

SF 001 03 01, Task 8104
(NEL N1-1)

This card is UNCLASSIFIED

Navy Electronics Laboratory
Report 1161

MACOMATIC CORRELATION SIGNAL PROCESSING SYSTEM, by W. B. Allen and C. E. Persons 40 p., 14 March 1963.

UNCLASSIFIED

A magnetic core matrix time compressor (MACOMATIC) has been developed for incorporation into a pseudorandom-signal-correlation sonar system. The MACOMATIC features a highly flexible input sampling rate -- any rate of up to 400 bits per second -- and a storage capacity of 2048 bits. Special timing pulses in the core matrix permit Doppler correction by adding or subtracting bits of information to effectively compress or expand the stored signal. The MACOMATIC is recommended particularly for use with spectrum analyzers for investigating low and very-low frequency phenomena.

1. MACOMATIC
2. Sonar signals - Processing

I. Allen, W. B.
II. Persons, C. E.

SF 001 03 01, Task 8104
(NEL N1-1)

This card is UNCLASSIFIED

THE PROBLEM

Make theoretical and experimental investigations to determine optimum techniques for generation, transmission, and reception of underwater acoustic signals. Specifically, develop a signal time compressor with a highly flexible input sampling rate and incorporate it into a correlation sonar system.

RESULTS

A magnetic core matrix time compressor has been developed and incorporated into a pseudorandom-signal-correlation sonar system. This magnetic core matrix time compressor can have any sampling rate of up to 400 bits per second and has a storage capacity of 2048 bits.

Special timing pulses were provided in the core matrix to permit Doppler correction by adding or subtracting bits of information at appropriately spaced intervals to expand or contract the reference waveform of the reference signal in time.

RECOMMENDATION

Apply the magnetic core matrix time compressor to correlation systems and spectrum analyzers for research signal processing, particularly in investigating low and very-low frequency acoustic, oceanographic, and seismic phenomena.

ADMINISTRATIVE INFORMATION

Work was performed under SF 001 03 01, Task 8104 (NEL N1-1). This report was approved for publication 14 March 1963.

CONTENTS

TABLES

ILLUSTRATIONS

INTRODUCTION

Echo-ranging systems employing correlation techniques require an artificial delay in the comparison signal to match the travel time of the received signal. In wide-band systems, artificial time delay can only be varied very slowly to maintain an adequate averaging time when passing through the region of signal match; thus long periods of time are required to search relatively small range intervals. To shorten search time, the system must use some form of multi-channel or compressed time signal processing.

This report covers the basic concept, operation, and instrumentation of a Magnetic Core Matrix Time Compressor (MACOMATIC) and its incorporation into a pseudo-random-signal-correlation sonar system. MACOMATIC belongs to the family of Scanned Storage Time Compressor (SCASTIC) systems that achieve time compression by a high-speed scan of signal storage elements, in contrast to those systems which achieve time compression by a high recirculation rate of the signal through the storage element, such as the Delay Line Time Compressor (DELTIC).[1]

The MACOMATIC correlation system is similar to equipments previously reported[2,3] except for the method of achieving the required time compression. In this system, as well as in those previously reported, a band-limited received signal is heterodyned to the near-zero frequency region, then clipped, sampled, time compressed,

---

[1] Harvard University. Acoustics Research Laboratory Technical Memorandum 37, DELTIC Correlator, by V. C. Anderson, 5 January 1956

[2] Westerfield, E. C., Rapid-Correlation Echo-Ranging System, U. S. Patent 3,046,545, 24 July 1962

[3] Navy Electronics Laboratory Report 1147, A Pseudorandom Signal Correlation System for Underwater Acoustic Research, by R. M. Zarnowitz and others, CONFIDENTIAL, 27 November 1962

and compared bit by bit with a reference signal which has been similarly processed except for a small (compared with signal bandwidth) "principal difference frequency" in the heterodyning process. ("Principal difference frequency" is defined later.)

This MACOMATIC has two unique features which make it a useful instrument for laboratory tests of the effect of sampling rate on signal-to-noise processing gain, and for evaluating a method of Doppler correction using bit compression techniques. The first of these features is the ability to sample at any rate of up to 400 bits per second by changing the frequency of the master clock. This flexibility permits the same time compressor to be utilized in correlation and spectrum analysis of very-low-frequency internal waves of the ocean, seismic waves, and sonar signals. The second feature is the ability to omit or repeat bits in the output sequence at selected times, thereby effectively compressing or expanding the stored signal.

MACOMATIC CONCEPT

Time compression can be achieved with a sequential access core memory[4] by writing the information into the cores at a low rate, $1/T_{is}$, and reading the information from the cores at a high rate, $1/T_{os}$, where T_{is} is the input-sample period and T_{os} is the output-sample period. If the input-sample rate is to continue without interruption and the output (in an interval T_{is} seconds) is to be a high-speed replica of the last N input samples, the writing of new samples and the reading out of stored samples must be interlaced so that $T_{is} = NT_{os}$, where N is the storage

---

[4] Huskey, H. D. and Korn, G. A., Computer Handbook, Section 12.7-18, McGraw-Hill, 1962

capacity in bits. The way in which the interlaced read-and-write operations are carried out will depend on the characteristics of the memory being used, the input-sample rate, and the number of signal samples to be stored.

Two modes of operation are required for a MACOMATIC to be used in a correlation sonar system: a static or storage mode, and a shifting or loading mode. The static mode, used to store the comparison signal, is the same as the read-and-restore mode of a sequential access buffer; that is, the information is read from the cores and, if necessary, restored in sequence without the addition of new signal samples. The same output waveform is repeated every T_{ts} seconds while the MACOMATIC is in the static mode. In the shifting mode, during which signal samples are loaded into the memory, a new signal sample enters every T_{ts} seconds and the oldest stored sample is simultaneously discarded. During the other $(N-1)$ read-pulse periods, all stored samples are read out and, if necessary, restored to the memory so that each stored sample appears every $(N-1)$ read pulses, and during each input-sample period (T_{ts}) the output waveform is a sped-up replica of the latest N signal samples.

Commoner magnetic core memories have destructive read-out,[5] requiring each bit of information which has been read out to be rewritten into the memory if it is to be retained. In this type memory, it is easier to implement the two modes of operation by (1) advancing the information one core for each time it is rewritten into the memory, for the shifting mode, and (2) rewriting it into the same core from which it was read, for the static mode. In this implementation a write pulse follows each read pulse. However, for an N-core memory every Nth write pulse will inject a new signal sample into the memory during operation in the shifting mode. If, each time all the stored samples are read out, the new signal sample is injected

---

[5] Huskey, H. D. and Korn, G. A., Computer Handbook, Section 12.7.7-.9, McGraw-Hill, 1962

into the last core addressed, the output waveform will be a sped-up replica of the input. If a new sample is injected into the first core addressed, the samples will appear in reverse order on the output.

MACOMATIC INSTRUMENTATION

The most direct instrumentation of a MACOMATIC for a memory with destructive read-out is a single-plane memory, providing T_{OS} is greater than the access (read-write) time of the magnetic-core memory. A single-plane MACOMATIC, as illustrated in figure 1 for a 4 × 5 matrix, consists of an array of square hysteresis-loop magnetic cores with X and Y address lines, sense line, inhibit line, X and Y address registers, sense amplifier, output register, Z driver, and control logic. Each row of cores is threaded by a Y address line, and each column of cores is threaded by an X address line. The core at the intersection of energized X and Y lines will be addressed. The inhibit line which threads all cores determines whether a "one" or a "zero" is written into the addressed core during the write cycle. The sense line which threads all cores will detect the information read-out of the addressed core during the read operation. The X and Y address registers select the order in which the cores are addressed. The control logic gates a signal sample from the output register, or the signal input to the Z driver, to be written into the memory. The output register holds the output information for two read-write cycles.

Each address register has a single "one" recirculating in it. The combination of these two "ones" addresses the memory in the following order: read 1, write 20, read 2, write 1, - - - read 20, write 19. The oldest stored sample is in core No. 1 and the newest sample is in core No. 20.

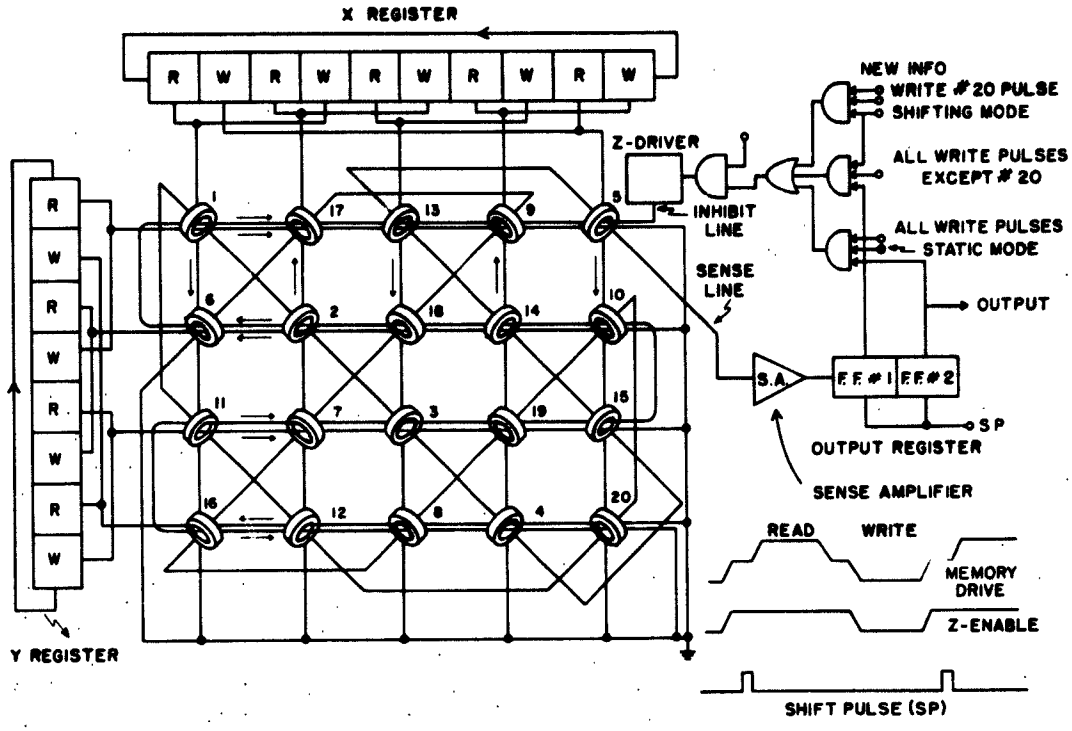


FIGURE I SINGLE PLANE MACOMATIC

With this read-write address sequence (R_1, W_{20}, R_2, W_1, - - - - R_{20}, W_{19}), the static mode of operation is obtained by taking the input to the *Z* driver from the second flip-flop of the output register. The signal samples appear at this point one read-write cycle after they are read from the memory; hence, they are written into the same core from which they were read.

The shifting mode is achieved by taking the input to the *Z* driver from the first flip-flop of the output register so that the signal sample is available to be rewritten into the memory with an advance of one core on the write portion of the same read-write cycle. Thus, after 20 read-write cycles, the oldest bit of information (that which was in

core No. 1) has been discarded, all the stored samples have appeared at the output and have been rewritten into the memory advanced by one core, and a new sample has been entered in the 20th core. During succeeding groups of 20 read-write cycles, all the stored samples advance one core in the memory so that after 400 read-write cycles a stored sample will have traversed completely through the memory and been discarded.

To obtain a given input-sample rate of $Q_{ts} = 1/T_{ts}$, the required access time T_A of the memory -- that is, the time required to complete a read-write cycle -- is equal to the signal-sample period T_{ts} divided by the storage capacity of the memory N: $T_A = T_{ts}/N$.

The access time of most readily available commercial magnetic core memories is 5-10 microseconds, while some late-model magnetic core memories have access times of 1 microsecond and thin-film magnetic memories have access times of approximately 0.1 microsecond. These storage elements will provide maximum input sample rates of 100, 1000, and 10,000 bits per second, respectively, for a storage capacity of 1000 bits.

The sampling rate for a system using a given type of storage element can be increased by operating n planes in series parallel. This is basically a modified sequential access memory with m words or characters and n bits per word. The minimum sampling period of such a system is $T_{ts} = T_A m = T_A mn/n = T_A N/n$ which corresponds to n times the sampling rate of the equivalent single-plane memory. In the loading mode only, one new signal sample is added to the memory each time the contents of the memory are read out and restored (one memory scan); thus all the stored samples appear at the output between the addition of new samples.

One method of achieving this is shown in figure 2. Although this equipment setup appears quite different and much more complex than the single-plane MACOMATIC, it is essentially n single-plane memories operating in

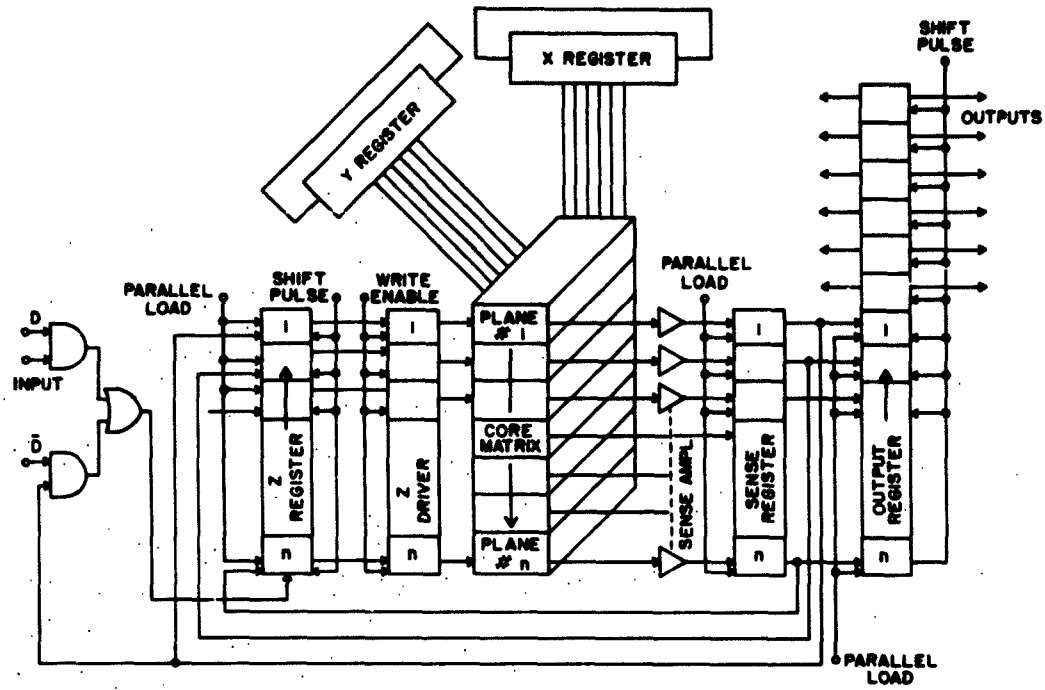


FIGURE 2 BLOCK DIAGRAM OF SERIES-PARALLEL MACOMATIC

parallel. The X and Y address registers are common to all n planes and produce the same read-write sequence as in the single-plane MACOMATIC: R_1, W_m, R_2, W_1, R_3, W_2, . . . R_m, W_{m-1}, R_1, W_m, etc. Each plane has its own sense amplifiers and Z drivers which operate essentially the same as in the single-plane MACOMATIC. Because the output register must shift serially n times during each read-write cycle, it cannot be used to store the information read from the memory on one read-write cycle until the next cycle. The n-stage sense register with parallel input and output is a buffer storage between the sense amplifiers and both Z and output registers. The n-stage Z register has parallel input and output plus serial shifting. The n+6-stage output register has parallel input and serial output. For the static mode, the read and restore operation is the same as for n single-plane MACOMATICS in parallel. The sense and

Z registers operate as n two-stage shift registers with the input to the Z drivers taken from the second stage. The separate output register receives the parallel outputs of the n-stage sense register and shifts them out serially before the next n bits are read from the memory. Thus each stored sample is rewritten into the same core from which it was read, and the output is a sped-up replica of the stored signal.

One method of instrumenting the shifting mode of operation is shown in the flow diagram of figure 3. The

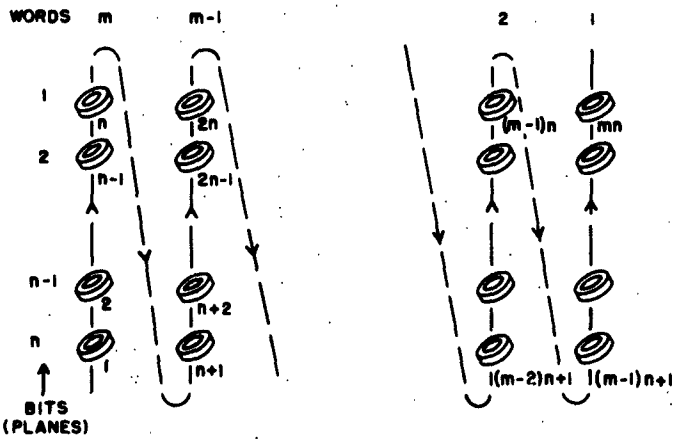


FIG. 3 FLOW OF SIGNAL SAMPLES IN MACOMATIC

new signal sample enters the memory at bit n of word m (core m of plane n) and shifts sequentially through each word in the memory until it reaches bit 1 of word 1 and is discarded. The number beside each core indicates the number of times the sample in that particular core has been written into the memory. Thus in n memory scans the signal sample moves sequentially from bit n to bit 1 of word m and on the next memory scan is written into bit n of word m-1. The signal sample continues moving

through the bit positions of each word until after mn memory scans it is in bit 1 of word 1 and is in position to be discarded on the next memory scan. This operation is accomplished by reading a word from the memory through the sense amplifiers to the sense register. At the start of the next read cycle, the signal samples in the sense register are transferred in parallel to the Z register and a new word is read from the memory into the sense register; thus two consecutive words are held in the Z and sense registers. Just before the start of the write portion of the read-write cycle, the first stage of the sense register and the Z register are shifted serially, transferring the signal sample from the first stage of the sense register to the nth stage of the Z register. The word rewritten into the memory consists of the last $(n-1)$ bits from the old word and the first bit from the sense register. When word n is in the Z register and the first word is in the sense register, the sample transferred into the nth stage of the Z register is taken from the signal input rather than the first stage of the sense register.

This selection of serial input to the nth stage of the Z register is made by the logic circuit shown in figure 4. The $\overline{D}$ signal enables the transfer gate to pass the output of stage 1 of the sense register to the last stage of the Z register at all times except during the "read 1" period. The D signal enables the transfer gate to pass the output of the Schmitt-trigger signal axis crossing selector (fig. 5) to the last stage of the Z register only during the "read 1" period. In this way, the oldest stored sample is replaced by a new signal sample to give an output signal which is a sped-up replica of the last NT_{ts} seconds of the input signal.

The output shift register shown in figure 6 consists of 14 stages (for instrumenting a series-parallel MACOMATIC with $n = 8$ planes and $m = 256$ words). The first eight stages are divided so locations 1, 3, 5, and 7 store the bits from the odd-numbered sense-register stages and locations 2, 4, 6, and 8 store bits from the even-numbered sense-register stages. All stages are shifted simultaneously

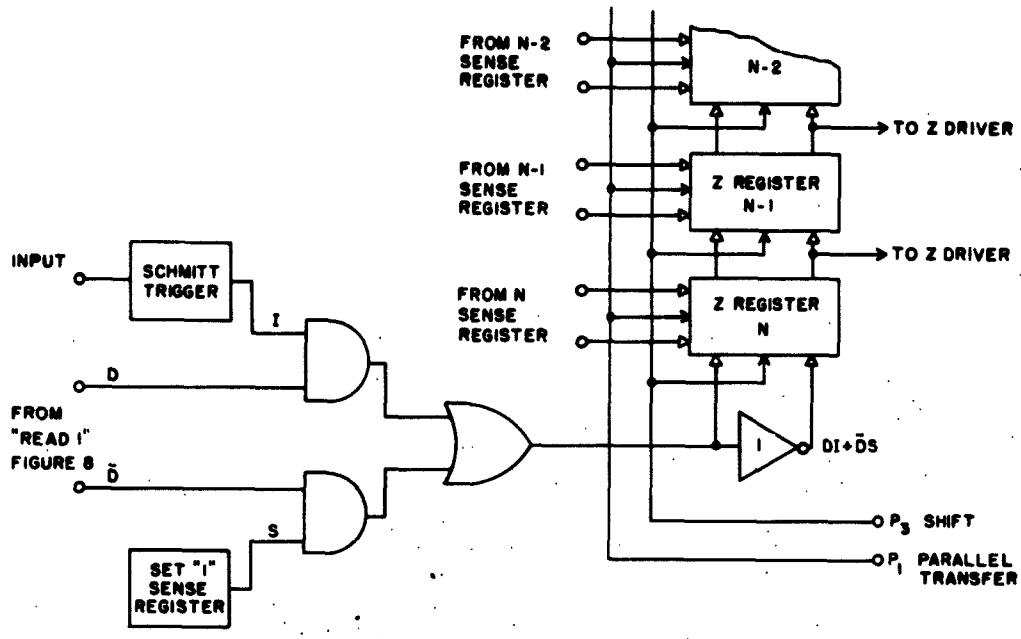


FIGURE 4 INPUT TRANSFER GATE

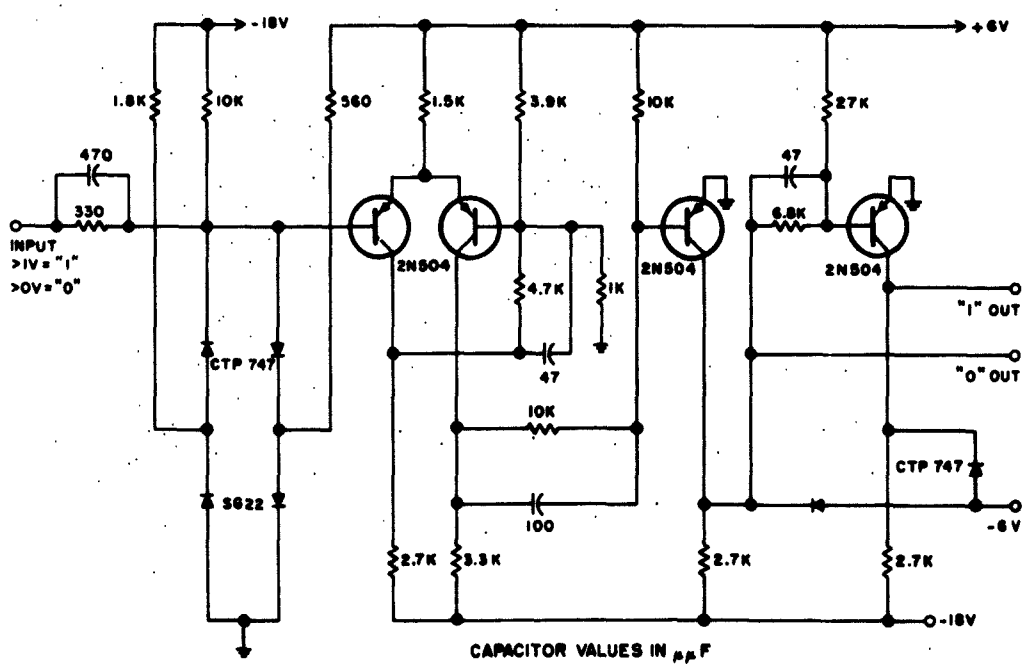


FIGURE 5 SIGNAL AXIS CROSSING SELECTOR (SCHMITT TRIGGER)

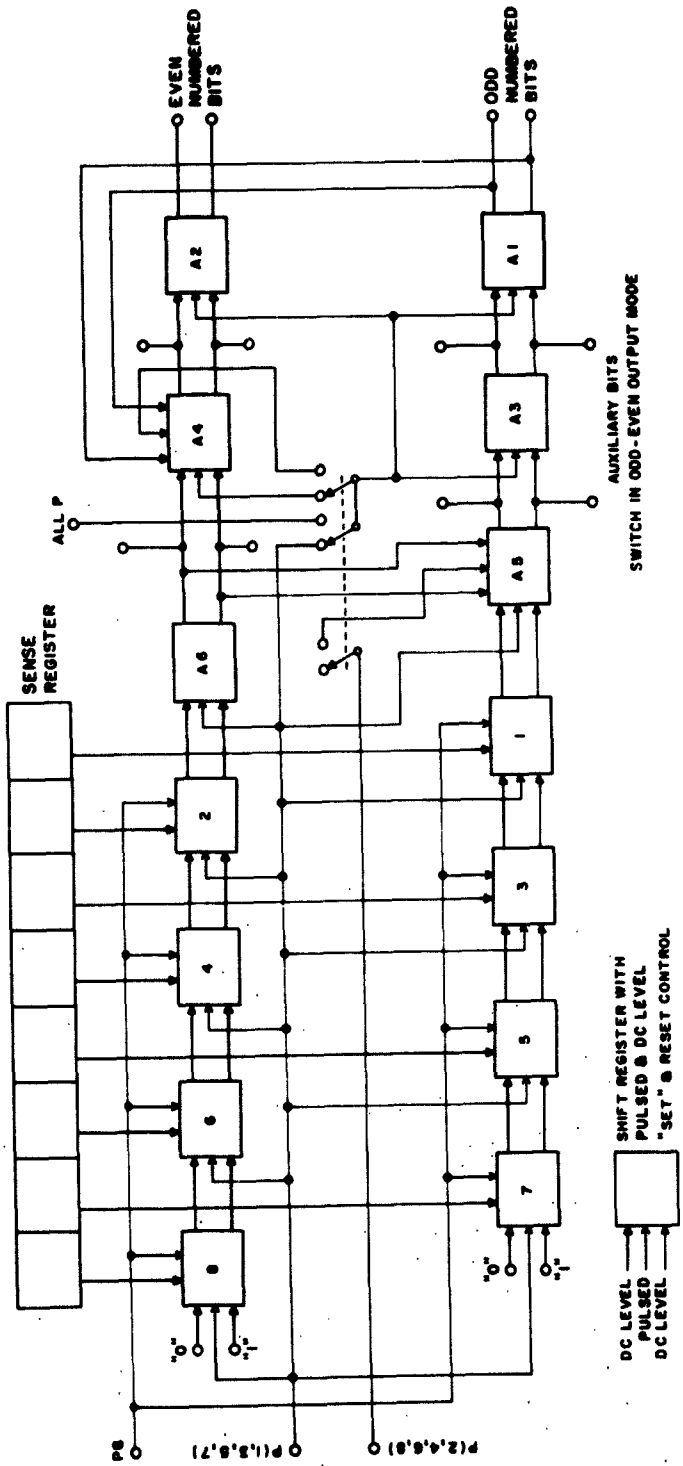


FIGURE 6 OUTPUT SHIFT REGISTER

at P_1, P_3, P_5, and P_7. The extra six stages(A_1, A_2, --- A_6) can be used in two different modes of operation. Three stages can be connected serially to the output of stage No. 1 and three stages to the output of stage No. 2 to present the odd-numbered bits and even-numbered bits separately at three different time delays (spaced T_{OS} seconds apart). Alternately, five of the stages can be connected serially with the sixth acting as a one-bit delay in the even-bit register output. The five extra stages are connected alternately to the odd and even registers so that all the bits shift through these five stages serially and in proper sequence. Extra delay in the even-bit register is required because the first eight stages are shifted at P_1, P_3, P_5, and P_7; thus the even bits are transferred out of stage No. 2 of the main register at the same time the odd bits are transferred out of stage No. 1 and they (the even bits) must be held in the extra stage until the next even-numbered clock pulse.

For a MACOMATIC with a maximum sample rate of 400 bits per second and a storage capacity of 2048 bits, the read-write cycle or access time for a single-plane MACOMATIC must be no greater than

$$T_A = \frac{T_{ts}}{N} = \frac{1}{4 \times 2.048 \times 10^5} = \frac{10^{-5}}{8.192} = 1.22 \text{ microseconds}$$

This is nearly eight times as fast as most readily available magnetic core memories can operate. Using eight planes in a series-parallel combination, the required access time is

$$T_A = \frac{T_{ts}^n}{N} = \frac{8 \times 10^{-5}}{4 \times 2.048} = 9.765 \text{ microseconds}$$

Timing details of the memory control, consisting of the read-write cycle, are shown in figure 7. The time required for one complete cycle is 9.765 microseconds which is divided into eight intervals by clock pulses occurring every 1.22 microseconds. The cycle starts with a

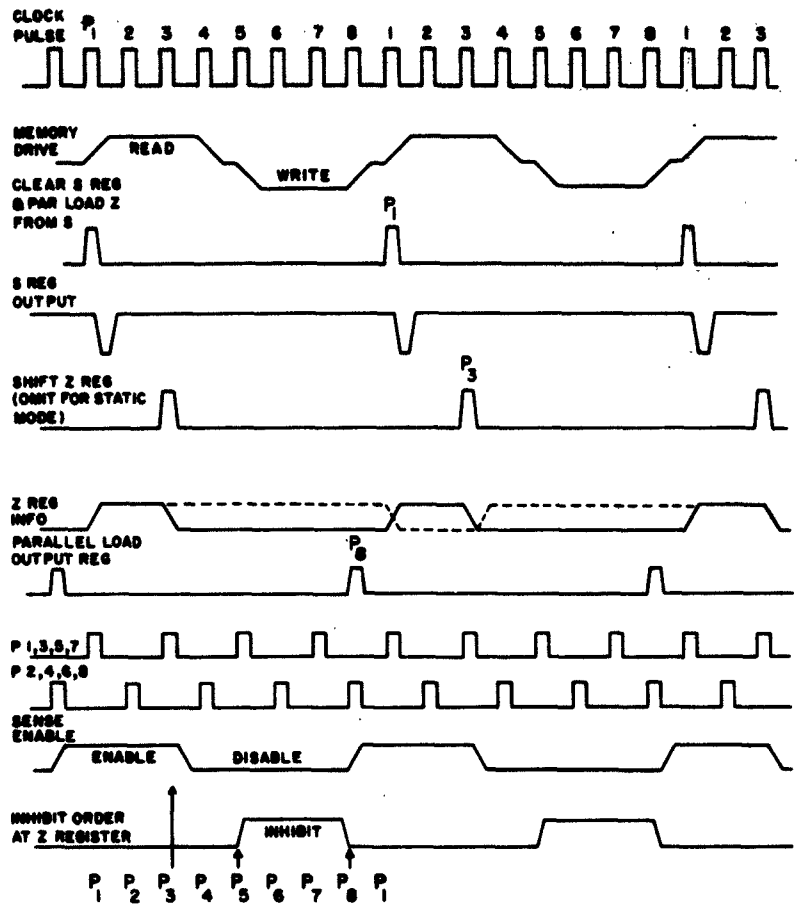


FIGURE 7 TIMING DIAGRAM

read operation and clear pulse to the sense register at P_1. Due to circuit delays in the core sense lines and amplifiers, the sense register flip-flops set approximately 1 microsecond after P_1. The samples are transferred to the Z register from the sense register as the sense register is cleared by the next P_1 pulse. The sense amplifiers are enabled during the read operation P_8 to P_3, and are inhibited during the write operation P_3 to P_8, so that switching of the cores during writing does not load false information into the sense register. In the shifting mode, a pulse

at P_3 shifts the Z register (advancing by one stage all bits of the old word) and transfers into the last stage of the Z register either the first bit of the new word in the sense register or a new signal sample. The write operation starts at P_5, the selected cores being addressed with a write pulse from P_5 to P_8, and the Z drivers being inhibited or enabled by the combination of outputs from the Z register and the inhibit-order-amplifier output pulse P_5 to P_8.

Mode Control

To change from the static to the shifting mode of operation, samples in the Z register merely are advanced one stage and the sample from the first stage of the sense register is shifted to the last stage of the Z register at P_3. The shift pulse at P_3 is generated by the advance gated clock driver which is controlled by the dc output of the mode control flip-flop as shown in figure 8. A switch on the front panel applies the correct voltage to force the mode control flip-flop into the static or shifting mode. A third position of this switch, AUTO LOAD, places the mode control flip-flop under control of the auto load flip-flop. In the static mode, the mode control flip-flop is held in the "zero" state so that the dc output level inhibits the input of the advance gated clock driver and no shift pulse is generated at P_3 to advance the Z register. In the shifting mode, the mode control flip-flop is held in the "one" state so that the dc output level enables the input of the advance gated clock driver, generating a shift pulse at P_3 to shift the Z register. In the "auto load" mode, the mode control flip-flop input gate is conditioned by the auto-load control flip-flop which is set by the externally supplied "start load" pulse. A magnetic-core transistor-logic-element counter produces an output pulse every 2048 "read 1" pulses. At the first pulse from this counter after occurrence of the "start load" pulse, the mode control flip-flop is set to the "one" state, transferring the memory to the shifting mode, and the auto-load control flip-flop is reset. The next pulse of this counter -- 2048 "read 1" pulses later -- resets the mode control flip-flop to the "zero" state, returning the memory to the static mode after the memory is filled with 2048 bits sampled from the signal input.

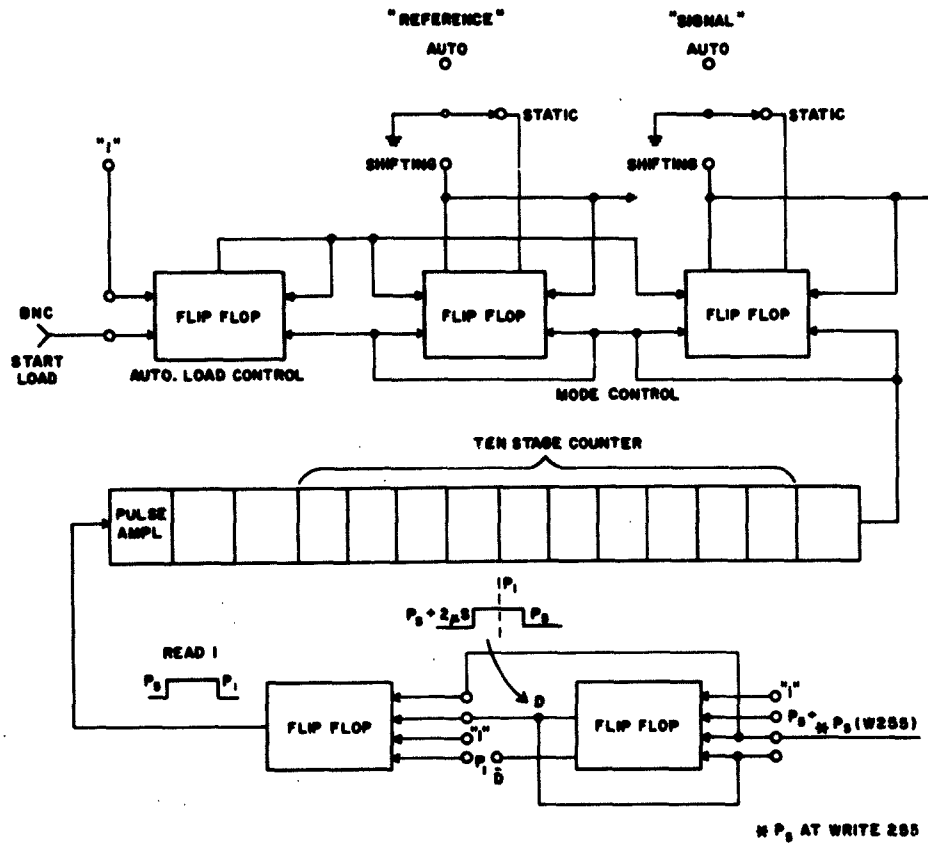


FIGURE 8. MODE CONTROL LOGIC

Timing and Control Pulse Generation

Control and timing signals required for operation of the memory are shown in figure 7. The output register must shift eight times during each read-write period; thus the basic clock frequency is eight times the access rate of the memory. The master clock signal is obtained from either an internal crystal-controlled oscillator or an external oscillator (fig. 9). A Schmitt trigger shapes the oscillator output to drive a gated clock driver which produces the master clock pulses. The clock pulses drive a three-stage binary counter to give a "divide by eight." Outputs of the three binary counter stages are combined logically in various gates and gated drivers (fig. 10) to produce the dc levels and pulses required to control operation of the MACOMATIC.

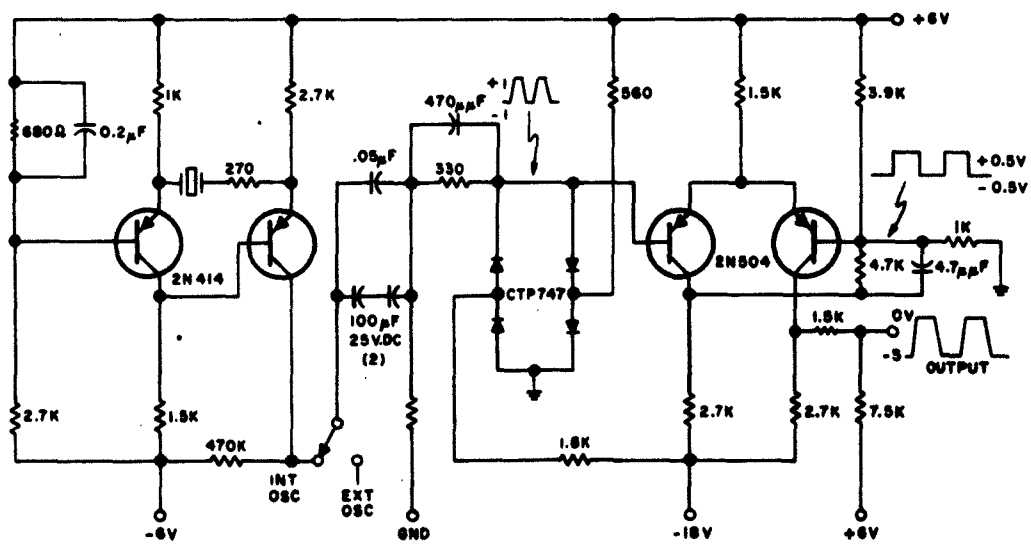


FIGURE 9 SCHMITT TRIGGER AND CRYSTAL OSCILLATOR

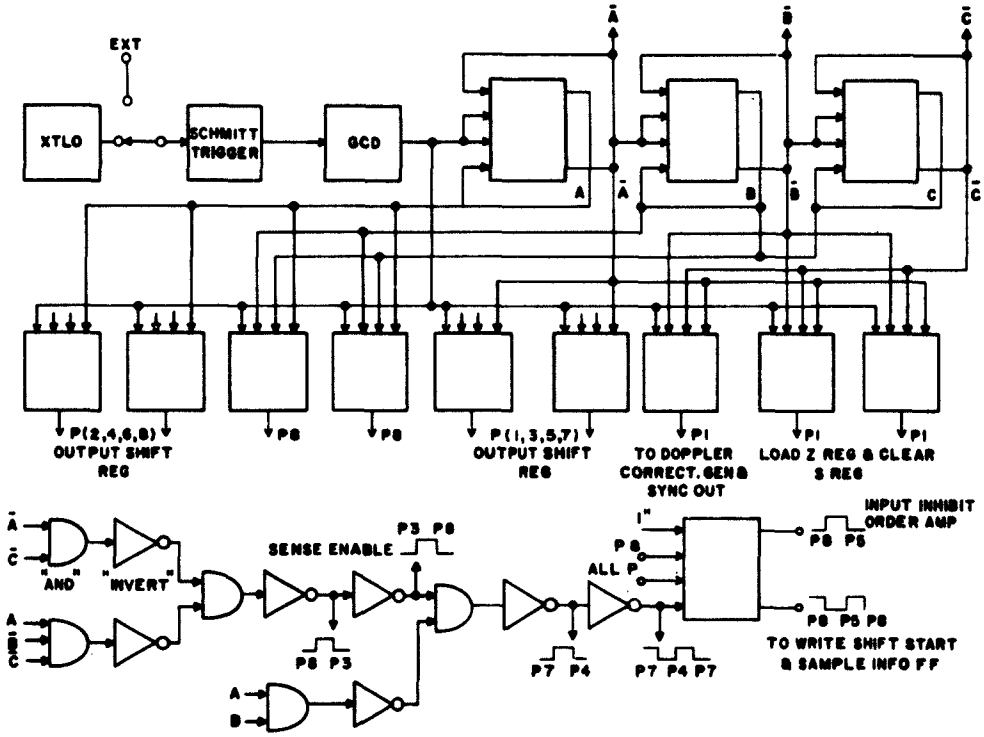


FIGURE 10. TIMING PULSE GENERATION

COMPLETE SYSTEM OPERATION

A block diagram of a MACOMATIC correlation system is shown in figure 11. The Shift Register Encoder[6] (SRE) (fig. 12), a 15-stage shift register with a modulo two adder in the feedback from the 15th and 14th stages to the first stage, generates a pseudorandom signal sequence which repeats every 10.24 seconds when the shift-pulse frequency is 3200 c/s. The SRE output is filtered to produce a signal band of from f_1 to f_2 c/s. The function of the double-position multiple pole relay (fig. 11) is to change the system from the transmit to the receive mode. In the transmit mode, the pseudorandom signal excites the power

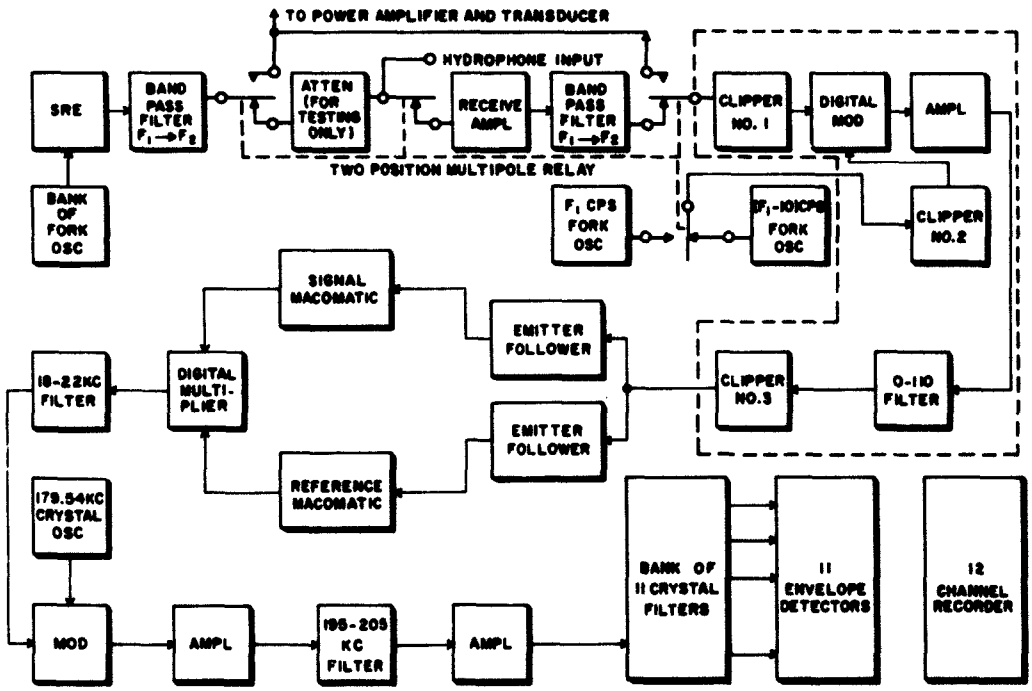
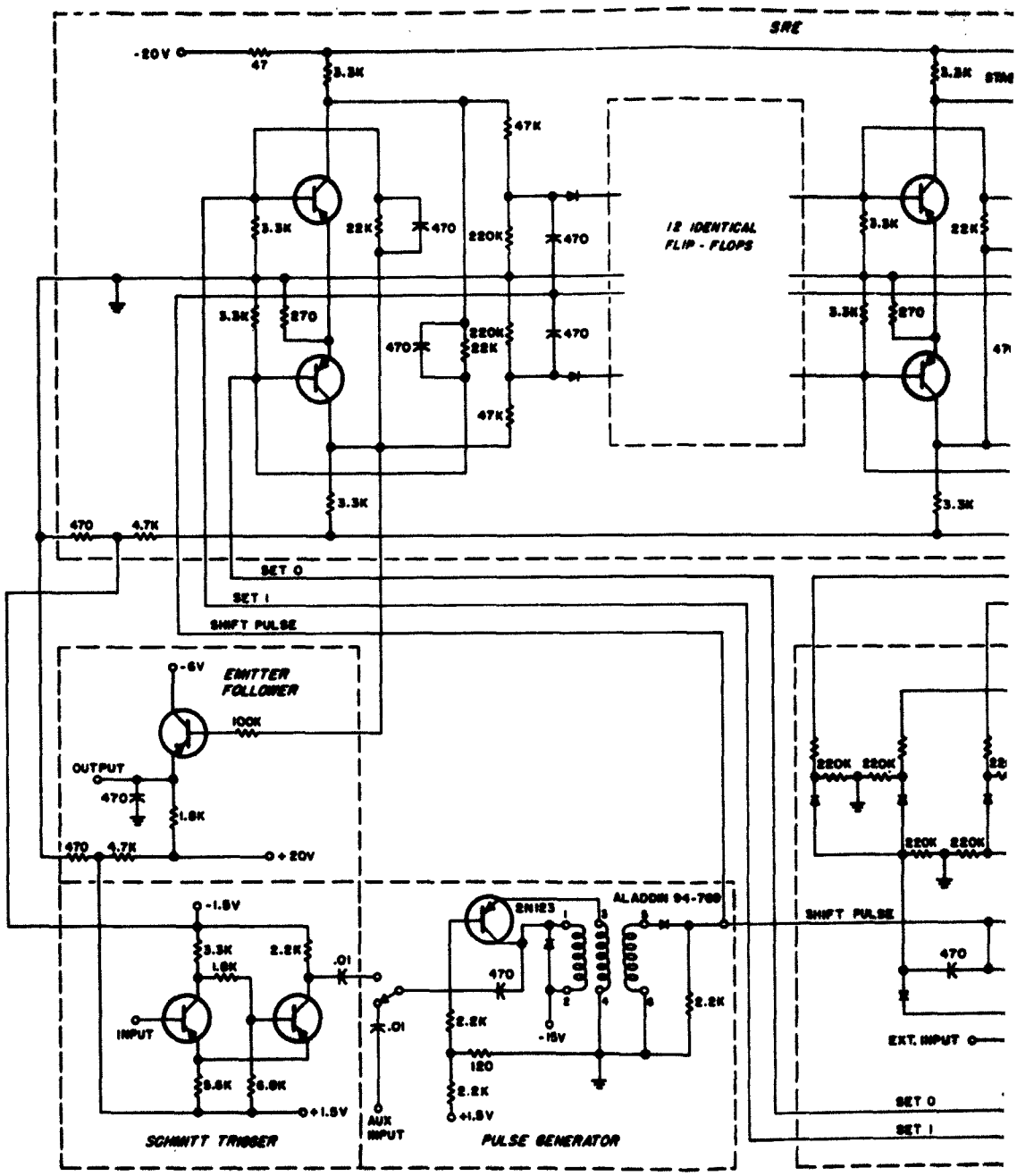


FIGURE 11 BLOCK DIAGRAM OF SYSTEM

[6] Green, J. H., Jr., and San Soucie, R. L., "An Error-Correcting Encoder and Decoder of High Efficiency," Institute of Radio Engineers. Proceedings, v. 46, p. 1741-1744, October 1958



NOTES:

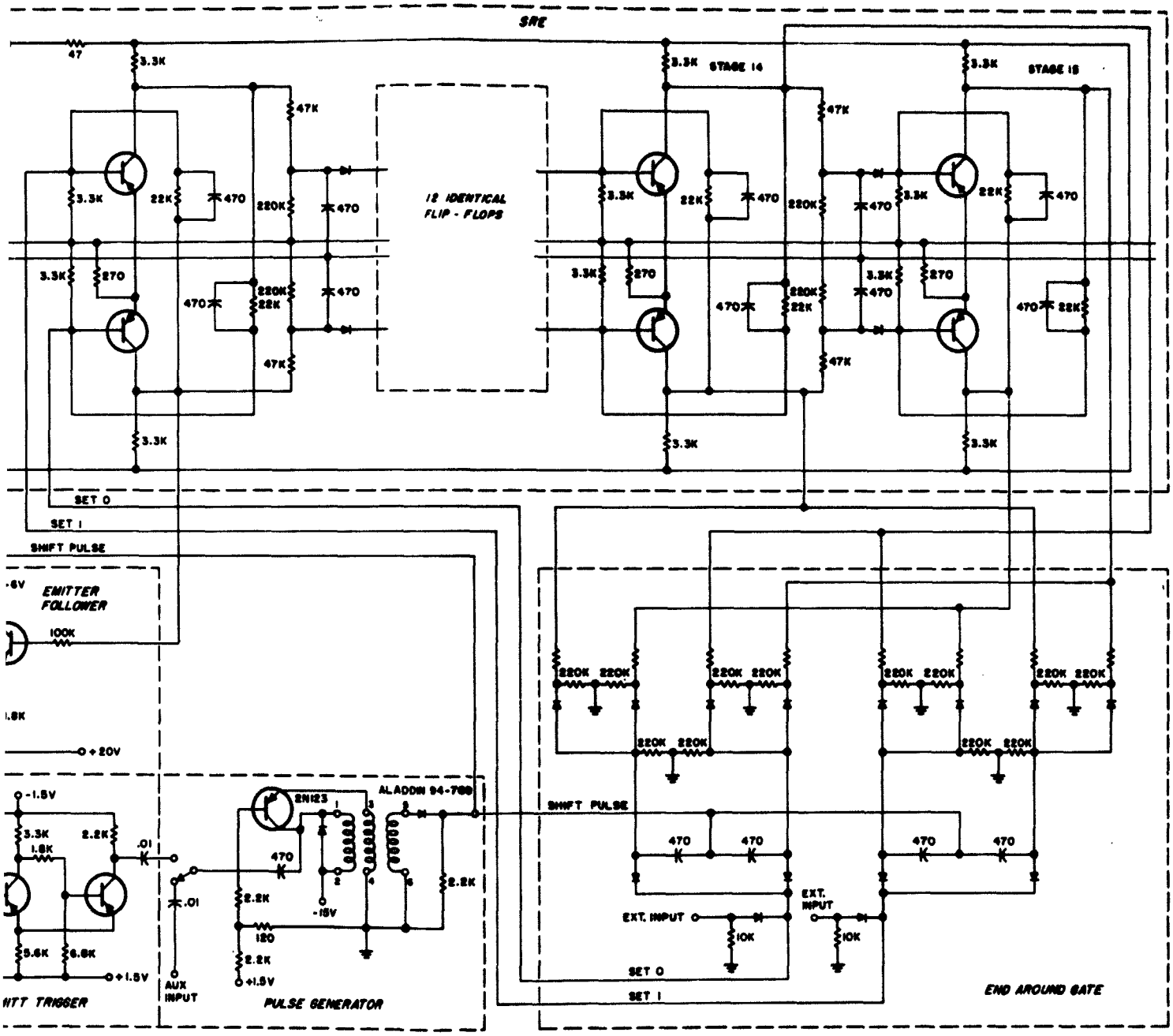
(1) ON 2 BOARDS:
- (A) 10 STAGES, EMITTER FOLLOWER, PULSE GENERATOR
- (B) 9 STAGES, END-AROUND GATE

(2) UNLESS OTHERWISE NOTED, ALL TRANSISTORS ARE 2N105

(3) ALL DIODES ARE IN ET7

(4) ALL CAPACITORS ARE IN $\mu\mu$F

FIGURE 12 SHIFT REGISTER ENCODER

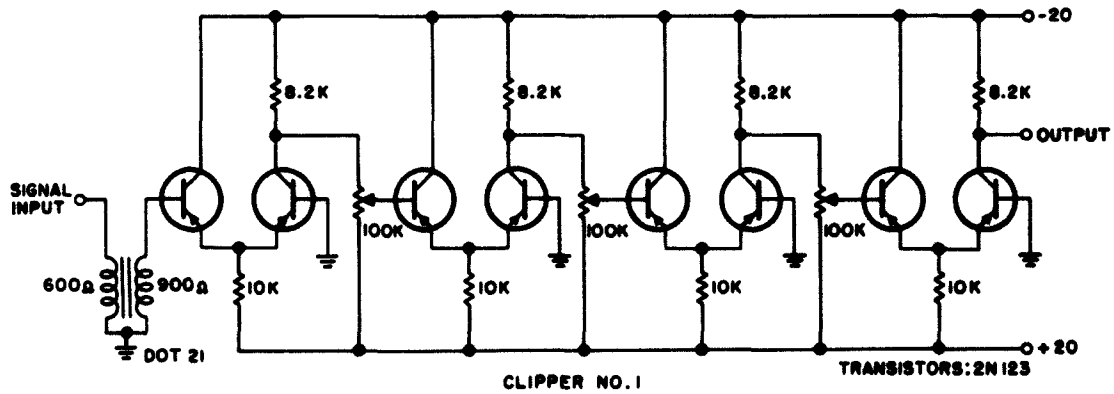


BOARDS:
10 STAGES, EMITTER FOLLOWER, PULSE GENERATOR
5 STAGES, END-AROUND GATE
ESS OTHERWISE NOTED, ALL TRANSISTORS ARE 2N105
DIODES ARE IN277
CAPACITORS ARE IN $\mu\mu$F

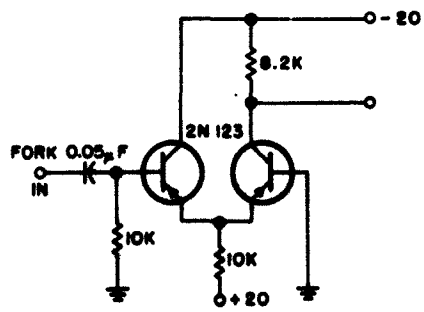
FIGURE 12 SHIFT REGISTER ENCODER

amplifier to drive the electro-acoustic transducer. Simultaneously, the band-limited pseudorandom signal is clipped, translated in frequency to a band at 0 to ($f_2 - f_1$) c/s, sampled, and stored in the reference MACOMATIC. In the receive mode, the output of the hydrophone is amplified, filtered, clipped, translated in frequency to a band at 10 to ($f_2 - f_1 + 10$) c/s, sampled, and stored in the receive MACOMATIC.

The components enclosed in the dotted lines in figure 11 are common to both modes of operation, the signals fed to them at any time being determined by the multicontact transmit-receive relay. The two clipper amplifiers, shown in figure 13, are emitter-coupled difference amplifiers. Clipper outputs provide the proper signal levels (-20 to 0) for the inputs to the digital modulator.



CLIPPER NO. 1



CLIPPER NO. 2

FIGURE 13 CLIPPERS

The digital modulator (fig. 14) performs the unsymmetrical denial logic operation ($AB + \bar{A}\bar{B} = 1$) on the binary level signals from the two clippers, which is equivalent to multiplication for the two-level signal + 1, - 1. The output of the modulator is amplified, low-pass filtered, clipped, and fed to two emitter followers which drive the input circuits of the receive and reference MACOMATIC's.

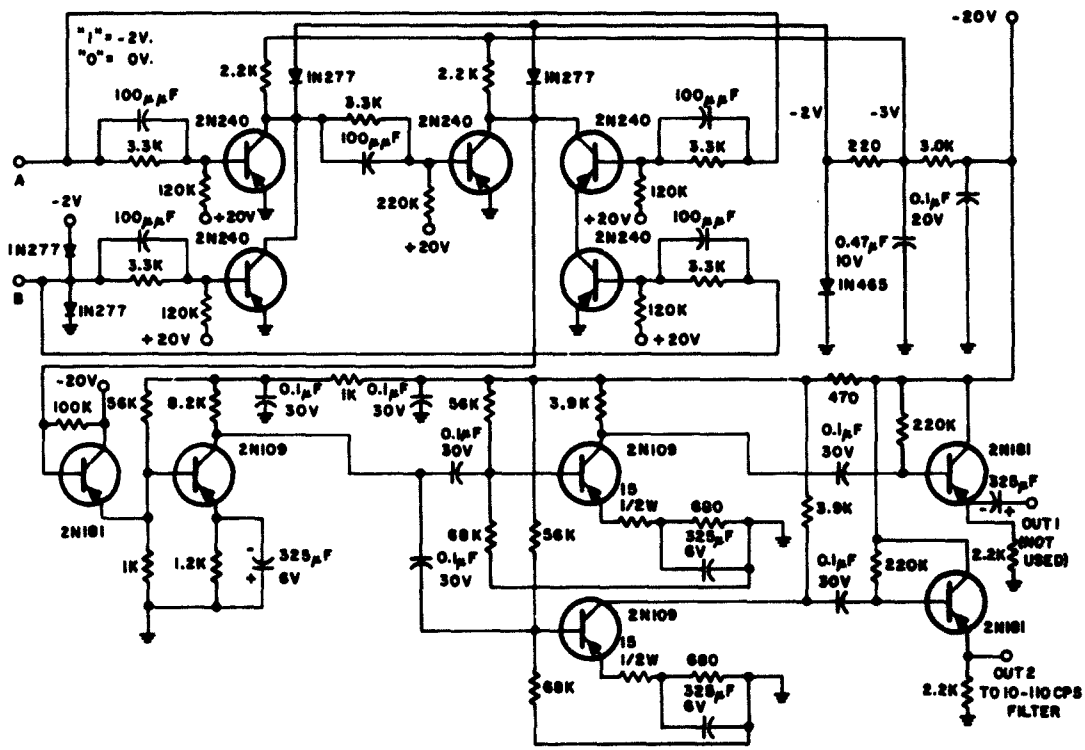


FIGURE 14 DIGITAL MODULATOR AND FILTER AMPLIFIERS

The inputs to clippers No. 1 and No. 2 during the transmit mode are, respectively, the band-limited signal from the SRE and the output of the f_1 c/s transistor-driven fork oscillator. The output of clipper No. 3, a clipped version of the 0 to($f_2 - f_1$) c/s signal band, sets the input Schmitt triggers of both magnetic core memories. After 2048 bits are stored in the reference memory, the

input is inhibited and each stored sample is read out of and restored to the same core in the memory without the addition of new information.

The input to clippers No. 1 and No. 2 during the receive mode are, respectively, the filtered output of the preamplifier shown in figure 15 and the output of the (f_1 - 10) c/s fork-controlled transistor oscillator. The output of clipper No. 3, a clipped version of the (10 to (f_2 - f_1 + 10) c/s signal band, sets the input Schmitt trigger of both MACOMATIC's. The receive MACOMATIC stores a new sample of the received signal every 2.5 or 5 milliseconds; after 2048 samples have been stored, the oldest stored sample is discarded as a new sample is added. The input to the reference MACOMATIC is inhibited during the receive mode of operation.

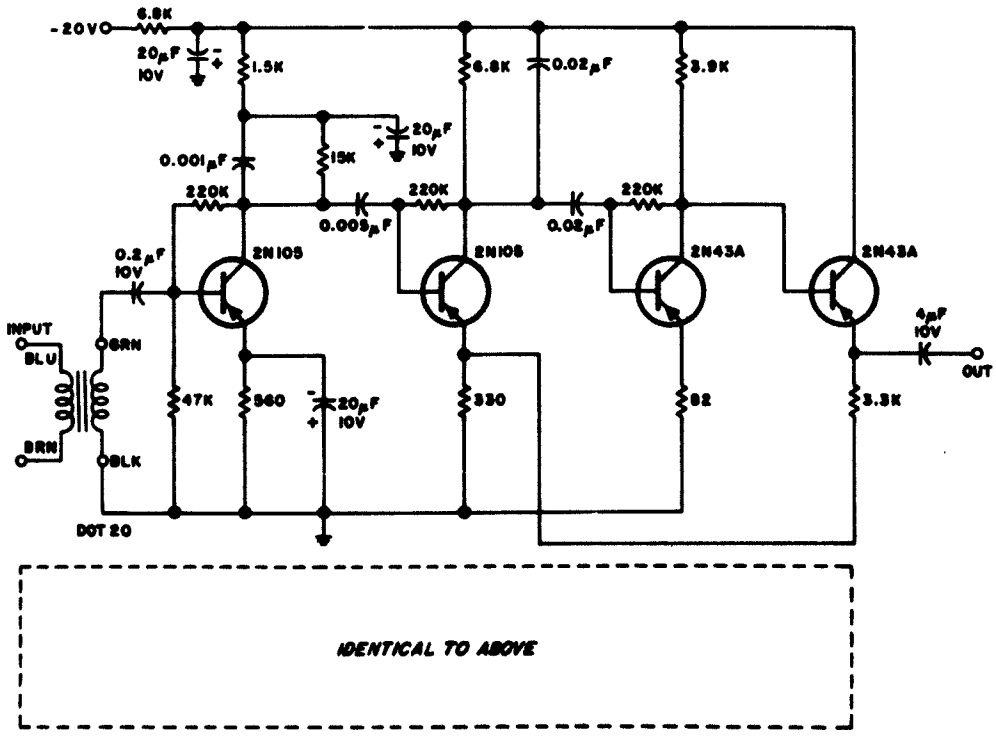


FIGURE 15 RECEIVER AMPLIFIER - TWO CHANNEL

The two MACOMATIC's are operated to read all 2048 cores during each sample period; thus the output sample rate is 2048 times the input sample rate. If, as in the static mode, the samples are read out and restored to the same core, a particular sample will appear at the output every input sample period T_{is}. If, as in the loading mode, the sample read out of core No. 1 is discarded, and the signal samples read out of cores 2, 3, 4, . . . 2048 (plus a new signal sample) are written into cores 1, 2, 3, . . . 2048, respectively, then a particular sample will appear on the output at regular time intervals $T_{is} - T_{os}$ for 2048 times, and then be discarded. The output of the receive MACOMATIC, operating in the loading mode, precesses one bit each sample period, with respect to the output of the reference MACOMATIC operating in the storage mode.

Each output sample of the receive MACOMATIC is multiplied by the time-coincident output sample of the reference MACOMATIC. Since the output samples of the receive MACOMATIC precess T_{os} every sample period T_{is}, each sample in the reference MACOMATIC output will multiply a different sample from the receive MACOMATIC during each sample period T_{is}. That is, as a new sample is read from the receive MACOMATIC for the first time, it is multiplied by the N^{th} sample in the reference MACOMATIC. $(N-1)$ sample periods later when this same sample is read out of the receive MACOMATIC, it is multiplied by the first sample in the reference MACOMATIC and discarded. By this process, the products of all time-coincident receive and reference samples for a given relative time delay are obtained, the relative time delay is changed by T_{os}, and the time-coincident products are obtained again. Any desired range of relative time delay (τ) can be covered.

The polarity coincidence circuit shown in figure 16 performs the logic function $SR + \bar{S}\bar{R}$ on the outputs of the MACOMATICS, where S and $\bar{S}$ are the outputs of the receive MACOMATIC while R and $\bar{R}$ are the outputs of the reference MACOMATIC. This is equivalent to multiplica-

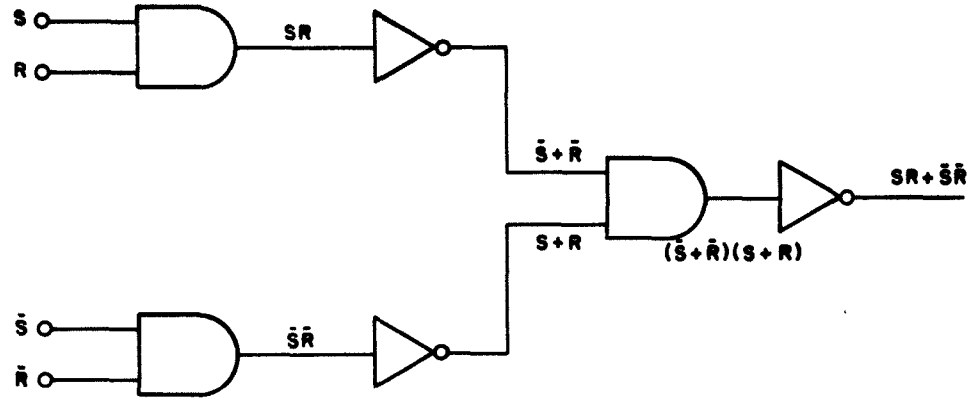


FIGURE 16 POLARITY COINCIDENCE LOGIC

tion for a binary level signal with "1" = 1 volt and "0" = -1 volt. This multiplication yields all the sum and difference frequencies for the two signals. It has been shown by Westerfield[7] that the spectrum will consist primarily of a series of bands whose width is equal to MACOMATIC input-signal bandwidth and whose centers are located φ_c c/s higher than multiples of $1/T_{is}$ c/s (where φ_c is the center frequency of the receive MACOMATIC input band). Amplitudes of the bands are governed by a $\left|\frac{\text{Sin } \pi f T_{is}}{\pi f T_{is}}\right|$ function centered on the sped-up "principle difference frequency" $N\varphi$, where $N = \frac{T_{is}}{T_{os}}$ and where, for the no-Doppler case, φ is the difference between the two frequencies used in the input heterodyning process. The components of a given band in the neighborhood $N\varphi$ will be in phase, resulting in a large

---

[7] NEL Technical Memoranda 279 (Part I, 1 April 1958) and 302 (Part II, 12 September 1958), A Theoretical Treatment of Cyclic Phenomena with Periodic Phase Discontinuities, by E. C. Westerfield, (internal publications)

amplitude for the output waveform when τ is close to zero (near peak correlation between the unheterodyned signals).

For this system, $N\varphi$ equals 2048 × 10 = 20,480 c/s; thus the band with the largest amplitude, for a sampling period T_{ts} equal to 5 or 2.5 milliseconds and with no Doppler shift on the received signal, is 20,410 to 20,510 c/s. After filtering to a bandwidth of 18.0 to 22.0 kc/s, modulation with the output of a 179,540-c/s crystal-controlled oscillator (fig. 17) translates this band to bands at 159,030 to 159,130 c/s and 199,950 to 200,050 c/s. The output of the modulator is amplified, filtered to remove the lower sideband, and passed to a bank of 11 crystal filters with center-frequency separations and 3-db bandwidths of 200 c/s. The output of each crystal filter is envelope-detected by the rectifier shown in figure 18 and recorded on a visicorder display.

A fractional Doppler shift, D, of the received signal will shift the center of the $\left|\frac{\sin \pi f T_{ts}}{\pi f T_{ts}}\right|$ function by approximately $\frac{f_1 + f_2}{2} ND$,

where $D = \frac{2 \text{ (velocity of target - velocity of transmitter)}}{\text{velocity of sound in the medium}}$.

Thereby, the amplitude of the zero-Doppler band is decreased and the amplitude of another band is increased. The position of the output in the filter bank is, then, an indication of the amount of Doppler as shown in table 1.

If Doppler becomes too large to be matched without compression or expansion, the reference signal can be compressed or expanded by changing the shifting frequency of the SRE and reloading the reference MACOMATIC. Doppler corrections obtainable by this method are shown in table 2.

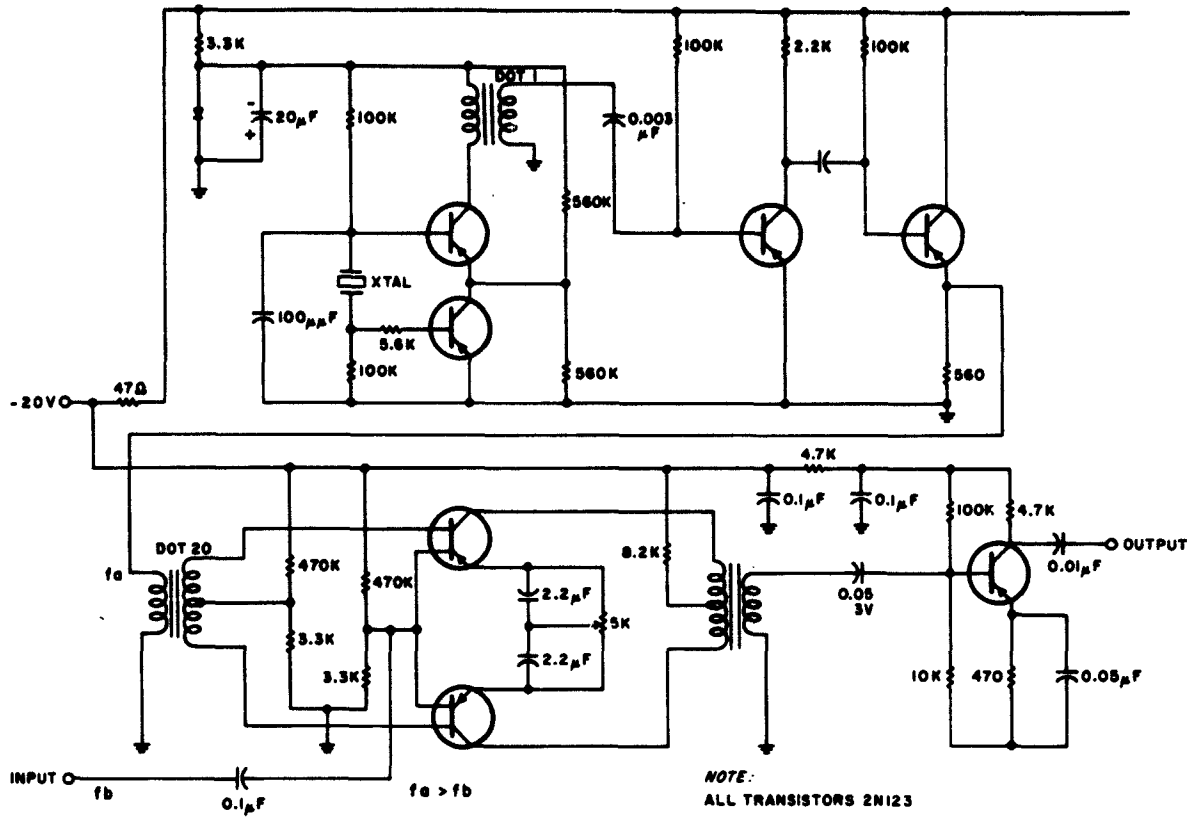


FIGURE 17 OSCILLATOR, MODULATOR AND CRYSTAL FILTER DRIVER

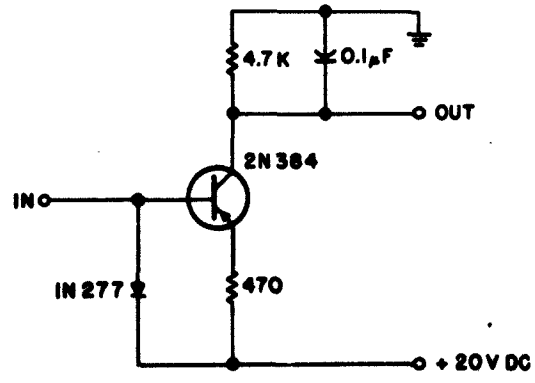


FIGURE 18 ENVELOPE DETECTOR

TABLE 1. DOPPLER INDICATION BY POSITION OF CORRELATION IN OUTPUT FILTER BANK.

FILTER CENTER FREQUENCY (kc/s)	DOPPLER FOR T_{ts} = 5 msec (knots)	DOPPLER FOR T_{ts} = 2.5 msec (knots)
199.00	-0.466	
199.20	-0.373	-0.373
199.40	-0.280	
199.60	-0.186	-0.186
199.80	-0.093	
200.00	0.00	0
200.20	+0.093	
200.40	+0.186	+0.186
200.60	+0.280	
200.80	+0.373	+0.373
201.0	+0.466	

TABLE 2. DOPPLER CORRECTION BY CHANGING SRE SHIFTING FREQUENCY.

SRE SHIFTING FREQUENCY (c/s)	DOPPLER CORRECTION (knots)
3196	-1.788
3197	-1.341
3198	-0.894
3199	-0.447
3200	0.0
3201	+0.447
3202	+0.894
3203	+1.341
3204	+1.788

In this system, up-Dopplers as great as approximately 1.4 knots could be processed in a filter bank with no decrease of component amplitudes for the output band of less than those at zero Doppler. For up-Dopplers greater than 1.4 knots or for down-Dopplers of any value, a decrease in amplitude for some components of the output band is to be expected. In general, the maximum number of filters which could be used to match up-Dopplers with no degradation of the spectrum is $2\left(T_{1s}\right)\left(f_o\right)$, where f_o is the center frequency of the transmitted signal.

SYSTEM TEST

A measure of processing gain against additive noise for this system was obtained by the test setup shown in figure 19. The amplifier gains were adjusted to make the signal RMS voltage V_1 equal to the noise RMS voltage, with the two attenuators I and II set at -4db; then the system output was recorded while V_1 was decreased. The results shown in figure 20 indicate that output correlations can be discerned 50 per cent of the time for an input-RMS-signal-to-noise ratio of -12 db. This is an indication of the improvement in detection capability, and is a measure of the processing gain when peak output signal is compared with peak output noise.

Processing gain is usually defined in terms of peak output signal to RMS output noise. This is obtained by setting $V_1 = V_2$ (RMS) and measuring the RMS value of the output noise and the peak amplitude of the output signal.

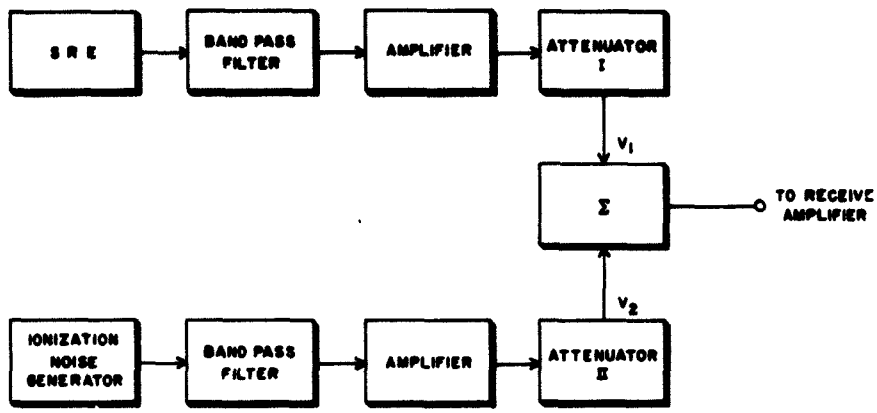


FIGURE 19. PROCESSING GAIN MEASUREMENTS

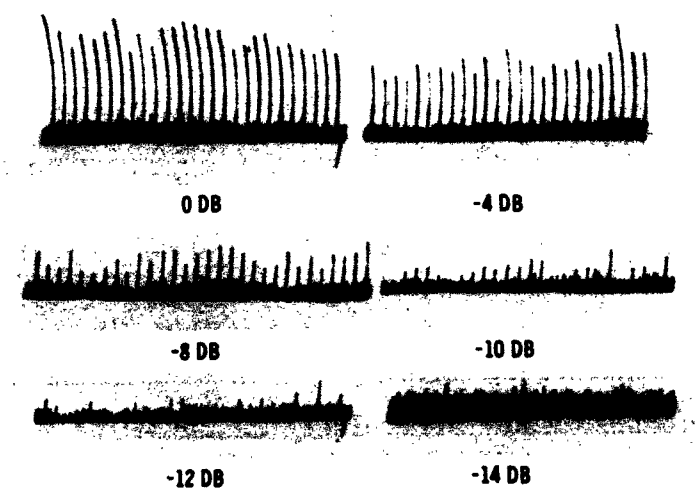


FIGURE 20 SYSTEM OUTPUT FOR VARIOUS INPUT-SIGNAL-TO-NOISE RATIOS (200-C/S SAMPLING)

The input-signal-to-noise ratio (RMS) is changed and the output noise (RMS) and output signal (peak) are again measured. Processing gain is equal to

$\frac{S_o/N_o}{S_I/N_I}$, with S_I, N_I, and N_o in RMS volts, and S_o in peak volts.

The results of these measurements are given in table 3.

TABLE 3. MEASUREMENTS OF PROCESSING GAIN FOR MACOMATIC SYSTEM WITH 200 C/S SAMPLING RATE.

INPUT (S/N) RMS (db)	OUTPUT S_{peak}/N_{rms} (db)	PROCESSING GAIN (db)
No Noise	26.1	
0	22.7	22.7
-4	19.7	23.7
-8	15.9	23.9
-10	12.8	22.8
-12	10.2	22.2

(Average = 23.1)

UNIQUE FEATURES AND TESTS

Sampling frequency of the system can be doubled by doubling the crystal clock frequency of the MACOMATIC from 409.6 to 819.2 kc/s. Figure 21 shows results of the processing-gain test with the 819.2-kc/s clock frequency. The sampling rate is 400 c/s, or four times the highest frequency of the MACOMATIC input band. Results show that the correlation spike can be discerned 50 per cent of the time for an input-signal-to-noise ratio of -12 db.

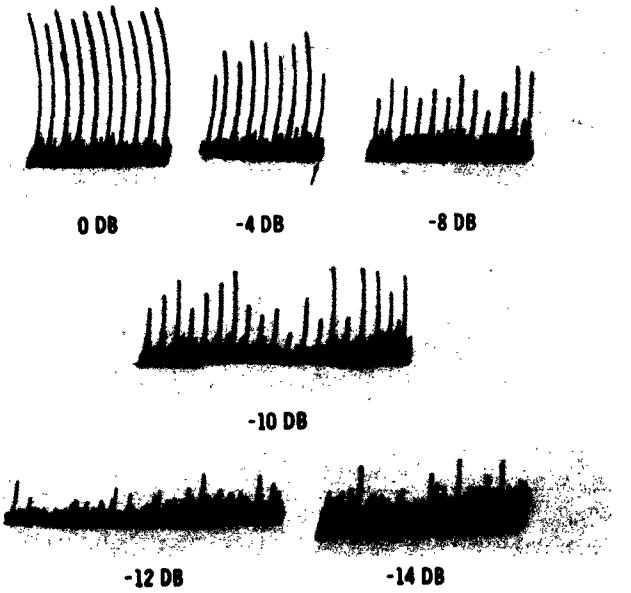


FIGURE 21 SYSTEM OUTPUT FOR VARIOUS INPUT-SIGNAL-TO-NOISE RATIOS (400-C/S SAMPLING)

Results of measuring processing gain against additive noise at a sampling rate of 200 c/s and storage time of 10.24 seconds are the same as for a sampling rate of 400 c/s and a storage time of 5.12 seconds. This indicates that one might expect an increase in processing gain at the higher sampling rate for an equal storage time. However, given a total number of bits of storage, it makes little difference as far as processing gain is concerned whether the sampling rate is twice or four times the highest frequency at the input to the MACOMATIC.

Bit Compression and Expansion

Another feature of the MACOMATIC is the bit compression (or expansion) technique for Doppler correction somewhat similar to that suggested by Westerfield[8]. The timing pulses (T_1, T_2 . . . T_{10}) shown in figure 22 are generated within the magnetic core equipment and brought to front connectors for easy access. By using these timing gates in conjunction with the extra stages of the signal and reference output registers and the polarity coincidence logic circuitry, reference output can be effectively compressed or expanded to match a small amount of signal-channel Doppler.

Table 4 shows an example of the logic used to compress or expand for various numbers of bits. S refers to signal-MACOMATIC outputs and R to reference-MACOMATIC outputs. The subscripts refer to the numbers of the six auxiliary flip-flops of the output register (A_1, A_2, . . . A_6) as indicated in figure 6.

---

[8]Navy Electronics Laboratory Report 698, LORAD Summary Report, Article 27, "Digital Techniques for Rapid Processing of Signals," p. vi-35, by E. C. Westerfield, CONFIDENTIAL, 22 June 1956

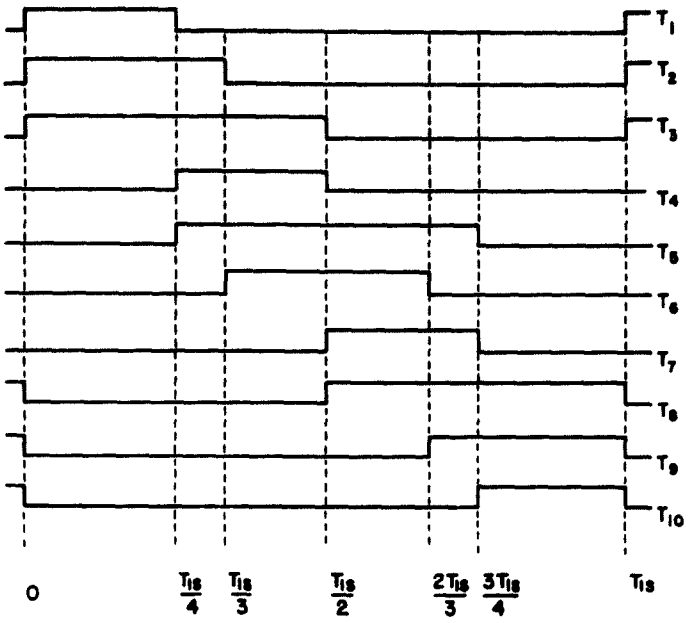
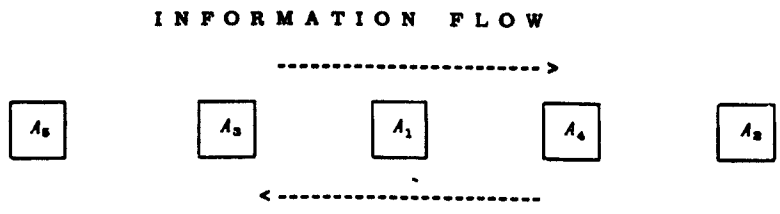


FIGURE 22. TIMING PULSES

For instance, to form an expansion of one bit, the logic indicates (1) performing a binary multiplication of the output of a signal register flip-flop with the output of any reference flip-flop for the first half of T_{ts}, then (2) multiplying the output of the same signal flip-flop with the output of a reference flip-flop which is delayed in time by T_{os} seconds (with respect to the reference output used in the first half of T_{ts}) for the second half of T_{ts}. An expansion of the reference-MACOMATIC output by one bit each recirculation is nearly equivalent to a compression of the signal-MACOMATIC output by the same amount.

A one-bit expansion or compression of the reference-MACOMATIC output will shift the center frequency of the spectrum-amplitude controlling factors for each component of the output bands by an amount proportional to the component frequency; i.e., for a 50-c/s MACOMATIC input frequency, center frequency shifts by 100 c/s, and for a

TABLE 4. LOGIC EQUATIONS FOR BIT EXPANSION AND COMPRESSION



COMPRESSION/ EXPANSION, NO. BITS	
0	$S_1R_1 + \overline{S}_1\overline{R}_1 = 1$
+1	$(S_1R_1 + \overline{S}_1\overline{R}_1)T_3 + (S_1R_3 + \overline{S}_1\overline{R}_3)T_6 = 1$
-1	$(S_1R_3 + \overline{S}_1\overline{R}_3)T_3 + (S_1R_1 + \overline{S}_1\overline{R}_1)T_6 = 1$
+2	$(S_1R_1 + \overline{S}_1\overline{R}_1)T_2 + (S_1R_3 + \overline{S}_1\overline{R}_3)T_6 + (S_1R_5 + \overline{S}_1\overline{R}_5)T_9 = 1$
-2	$(S_1R_5 + \overline{S}_1\overline{R}_5)T_2 + (S_1R_3 + \overline{S}_1\overline{R}_3)T_6 + (S_1R_1 + \overline{S}_1\overline{R}_1)T_9 = 1$
+3	$(S_4R_4 + \overline{S}_4\overline{R}_4)T_1 + (S_4R_1 + \overline{S}_4\overline{R}_1)T_4 + (S_4R_3 + \overline{S}_4\overline{R}_3)T_7 + (S_4R_5 + \overline{S}_4\overline{R}_5)T_{10} = 1$
-3	$(S_4R_5 + \overline{S}_4\overline{R}_5)T_1 + (S_4R_3 + \overline{S}_4\overline{R}_3)T_4 + (S_4R_1 + \overline{S}_4\overline{R}_1)T_7 + (S_4R_4 + \overline{S}_4\overline{R}_4)T_{10} = 1$

100-c/s MACOMATIC input frequency it shifts by 200 c/s. These are equivalent to shifts of $\frac{100}{2048}$ and $\frac{200}{2048}$ c/s, respectively, for MACOMATIC input frequencies, or for the center frequency and highest frequency of the echo band. However, since these shifts are not proportional to the corresponding frequencies in the echo band, bit compression or expansion of the reference-MACOMATIC output alone is not an exact Doppler correction scheme for this type of system because such compression or expansion corrects only for dispersion within the band and not for frequency translation of the band.

CONCLUSIONS

The flexible input-sample rate of the MACOMATIC results in a very flexible time compressor well suited to research signal-processing equipment. For low frequencies that do not require series-parallel operation, the memory-core planes can be operated in parallel to carry different signals, or they can carry the parallel outputs from an analog-to-digital converter to retain the signal amplitude information for correlation or spectrum analysis studies. The MACOMATIC can be implemented with sequential access buffer memories by the addition of extra registers and gating circuitry.

RECOMMENDATION

Apply the MACOMATIC to correlation systems and spectrum analyzers for research signal processing, particularly in investigating low and very-low frequency acoustic, oceanographic, and seismic phenomena.